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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
Chihiro Araki

App. No.:	10/063,869
Filed:	May 21, 2002
Conf. No.:	2434
Title:	INSPECTION METHOD AND INSPECTION APPARATUS FOR SEMICONDUCTOR CIRCUIT
Examiner:	T. Nguyen
Art Unit:	2829

Commissioner for Patents
Arlington, VA 22313-1450

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January 26, 2004
Ernest A. Beutler
Reg. No. 19901

APPELLANT'S BRIEF

There are no other Appeals or Interferences, that have a bearing on or which would be affected by the decision in this Appeal.

REAL PARTY IN INTEREST

In addition to the appellant, the real party in interest is his assignee, Kabushiki Kaisha Moric, a Japanese company.

STATUS OF THE CLAIMS

Claims 1 through 6 are present in this application. Claims 4 and 5 have been allowed. Although the Final Rejection lists these claims among those rejected, the Advisory Action, dated December 5, 2003, refusing to enter a proposed amendment after final indicates the status of claims 4 and 5 as being allowed. Therefore it is assumed that only claims 1 through 3 and 6 are before the Board on Appeal.

STATUS OF AMENDMENTS

As noted above, an amendment was filed in response to the final rejection but was refused entry as it allegedly "is a new issue in claim scope"; therefore, the claims on appeal are as finally rejected.

A clean copy of the appealed claims appears in the Appendix to this Brief.

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APPELLANT'S INVENTION

Appellant's invention relates to a method and apparatus for testing the components semiconductor circuit with a plurality of connected semiconductor devices that is simple and highly effective and which requires no individual or computer interpretation. If applicant's attorney will be permitted some poetic license, he would like to quote from the sole reference relied upon the Examiner in his final rejection of the claims on appeal. This is being done because the following quotation from the reference not only clearly states the problem with prior art methods and apparatus, but emphasizes the patentable distinction between the claims on appeal and the structure and method utilized by the reference.

Column 1, lines 40 through 68 of Spence et al 5,440,566 (Spence et al) state:

> "A recent alternative to guided probing and bed of nails testing has been the use of thermographic imaging. Infrared energy emitting from an operating PCB under test produces a unique thermographic image which can be compared with the image of a PCB that is known to be in good operation.
>
> A problem with existing infrared testing systems for PCB's is that the thermal images have required subjective interpretation by a skilled technician. These interpretation difficulties have prevented wide use of thermal information for ATE testing.
>
> Another problem with existing infrared red testing systems is that it is difficult to accurately determine the emissivity of the circuit board under test. Emissivity is a measure of a surface's ability to radiate energy, referenced to that of a perfect, or "blackbody" surface. To accurately determine the temperature of an object from measurements of radiated energy, the emissivity of the object's surface must be known. The problem of determining temperature is made more difficult when the object has areas of different emissivity, such as is the case with PCB's where the devices on the PCB may be plastic, ceramic, bare metal or treated metal. Even components of the same type may have different emissivities on different PCB's.
>
> A need exists for an improved, easy to use, method for producing and diagnosing thermographic images."

How Spence et al solves this stated problem and how that differs from appellants solution will be discussed in APPELLANT'S ARGUMENTS below. Basically the way appellant solves this problem is to apply a load to the circuit and then take a thermographic picture of the circuit board which is processed to determine the temperature of the semiconductor devices for determining the quality of circuit and its semiconductor devices based on the heat development rather than the temperature of the components itself. This is described in full detail by reference to the figures of the drawings in the appropriately headed portion of the specification.

THE ISSUE BEFORE THE BOARD

Since the claims before the Board have been rejected solely under 35 USC 102(b) on Spence et al, the only question before the Board is whether the claims are fully readable on this reference.

GROUPING OF THE CLAIMS

No two of the appealed claims stand or fall together and the patentability of each claim will be argued separately.

APPELLANT'S ARGUMENTS

At the beginning of this brief appellant quoted a section of the Background portion of the Spence et al patent to demonstrate that it was intended to address the same problem as appellant. It was also stated there that the solution suggested by reference is quite different from appellants as well as being much more complicated and expensive. That point will be developed more fully now and then the distinguishing claim language will be pointed out.

Spence et al acknowledges that the prior art methods and apparatus "required subjective interpretation by a skilled technician". His solution is basically to use the same technique as the prior art, but substitutes an " artificial neural network" for the skilled technician (see claim 1). In addition he requires the creation of "an emissivity map" and uses it to "correct said thermal image" (claim 1) . Then the result is delivered to the artificial neural network so that it "which has been previously trained" can make the interpretation previously made by the skilled technician.

Contrast this with appellant's invention which only requires the taking of a picture by a thermographic camera, processing that image to determine the temperature of the semiconductor devices and thus determining the quality of circuit and semiconductor devices based on the heat development. Obviously a much simpler and less costly solution to the problem.

Thus the question is whether these vast differences are pointed out in the claims and it is submitted that they are. Claim 1 clearly calls out the step of "taking a photograph of the circuit with a thermographic camera to detect heat development of each semiconductor device in response to the applied load". This photograph is then used to "determine the temperature of the semiconductor devices for determining the quality of circuit and semiconductor devices". The Spence et al reference never determines temperature from a thermal image. Rather it modifies the image it obtains to create an emissivity map that modifies the image and then that modified image is compared by the trained neural network to make a comparison with a normal image. How could the differences be greater?

Quite simply, a temperature of either a component nor the complete circuit is never determined in Spence et al. In addition claim 1 requires determination of "the quality of circuit and semiconductor devices based on the heat development". Spence et al does not do this contrary to the Examiners allegation because he only makes a visual comparison of the modified image with a normal image using the trained neural network. There clearly is no anticipation here. Appellant and Spence et al make their determinations in substantially different ways. The Examiner is challenged to point out a specific place in the reference where it refers to a temperature being detected. He can not because the reference only compares images not temperatures.

Claim 2 depends on claim 1 and thus partakes of this distinction. In addition it calls for the circuit being tested to have "at least some of the semiconductor devices connected in parallel". He alleges that Figure 1 of the reference shows this. Perhaps the Examiner sees this in that figure, but appellant's attorney can not see any circuit in this figure and it is seriously doubted that the Board will either.

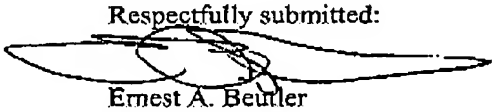
Claim 3 depends on claim 1 and further distinguishes over the reference in calling for the "temperatures of the semiconductor devices are measured at different points of time, and the quality of the circuit and semiconductor devices is determined based on the temperature difference". Again the Examiner incorrectly characterizes the disclosure of the reference by referring to the disclosure beginning at column 5, line 65 and ending at column 6, line 48. He alleges that X_0, Y_0 and X_n, Y_n are points of time. They are not. These are locations on the circuit board. But again the Board can itself see that the Examiner has apparently read appellants disclosure into the reference. The discussion in the refcrence here deals with the attempt to take the images when the circuit is in thermal equilibrium not at different temperatures.

Claim 6 is a separate independent claim and is drawn to the apparatus. The Examiner in his rejection refers to the components but not the functions they perform. The claim requires an "image processor connected to said thermographic camera for determining the temperatures of said semiconductor devices solely from the output of said thermographic camera". The reference does have an image processor, but as noted above it does not determine temperature from the camera output as already stressed above. The determination of "temperatures of said semiconductor devices solely from the output of said thermographic camera" is not taught or even suggested by the reference.

In fact in his advisory action of December 5, 2003, he stated that determining the result "based solely on the temperature measurement is a new issue". From this it is clear that he apparently did not even read this clear limitation as having already been recited in claim 6.

Thus it is believed that, even without the foregoing arguments, the Board can not reach any other conclusion that the Examiner has failed to make out a prima facia case of anticipation, because of the substantial differences both in methodology and structure between the claims and the disclosure of the reference. A reversal of his grounds of rejection is therefore respectfully requested.

Respectfully submitted:



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Attachment: Credit Card Authorization for Brief Fee

APPENDIX- CLEAN COPY OF CLAIMS ON APPEAL

1. An inspection method for a semiconductor circuit with a plurality of connected semiconductor devices comprising the steps of applying an electrical load on the circuit, taking a photograph of the circuit with a thermographic camera to detect heat development of each semiconductor device in response to the applied load, and processing the photograph to determine the temperature of the semiconductor devices for determining the quality of circuit and semiconductor devices based on the heat development.

2. The inspection method for a semiconductor circuit according to claim 1, wherein at least some of the semiconductor devices are connected in parallel.

3. The inspection method for a semiconductor circuit according to claim 1, wherein temperatures of the semiconductor devices are measured at different points of time, and the quality of the circuit and semiconductor devices is determined based on the temperature difference.

6. An inspection apparatus for a workpiece consisting of a semiconductor circuit with a plurality of connected semiconductor comprising an apparatus body on which a workpiece to be inspected is set, a loading circuit for applying load corresponding to the condition of use to the workpiece, a power source for supplying a working current to the workpiece through said loading circuit, a drive waveform generating circuit for applying a drive signal to said workpiece, a thermographic camera for taking photographs of the workpiece set on said apparatus body, an image processor connected to said thermographic camera for determining the temperatures of said semiconductor devices solely from the output of said thermographic camera, and a control for controlling said inspection apparatus to perform an inspection program